A Circuit-Based Approach to Efficient Enumeration

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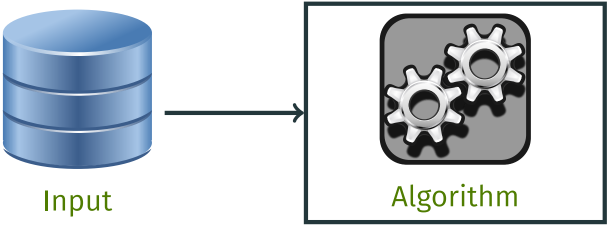
[4]CNRS CRIL

Problem statement

Problem: Enumerating large result sets

Input

Problem: Enumerating large result sets



Problem: Enumerating large result sets

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Algorithm

A	B	C
a	b	c
a’	b	c
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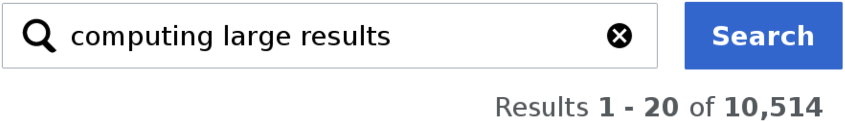

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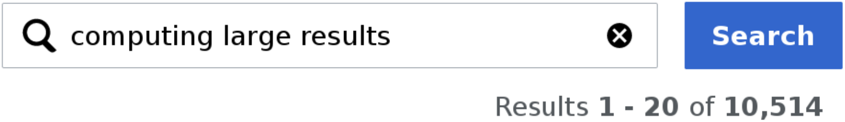

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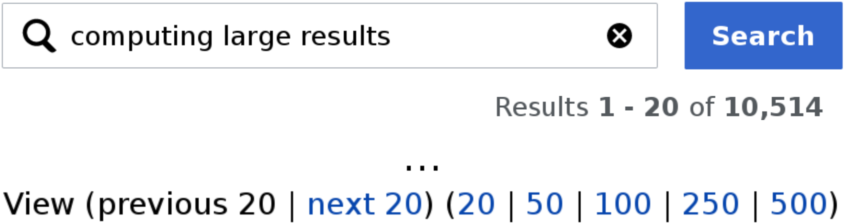

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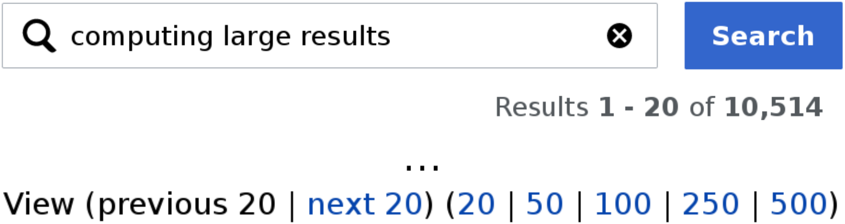

→ Solution: Enumerate solutions one after the other

Enumeration algorithm

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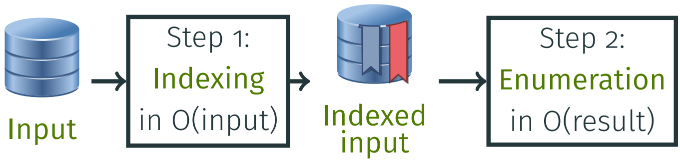

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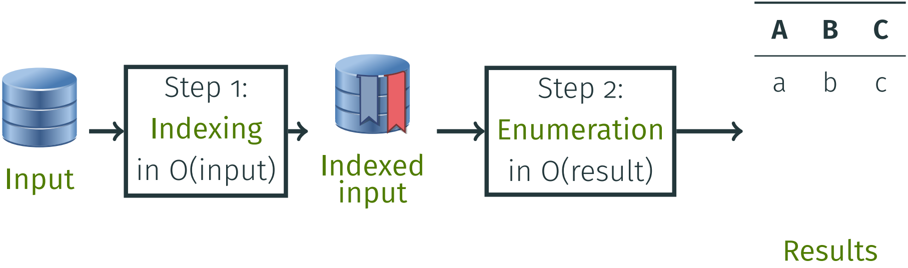

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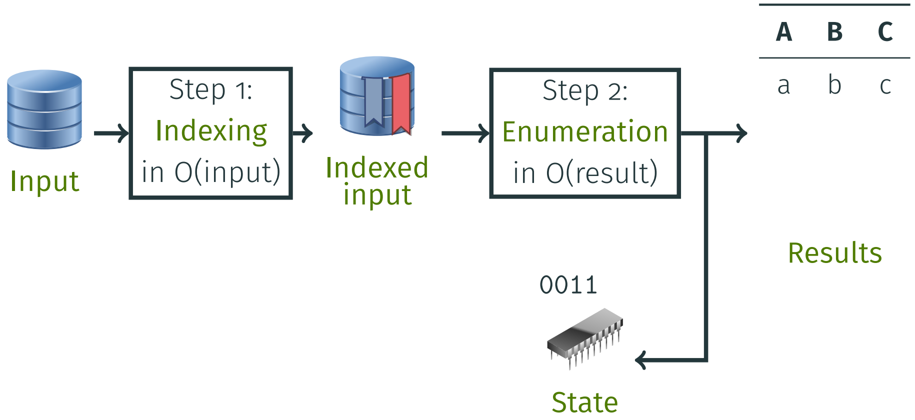

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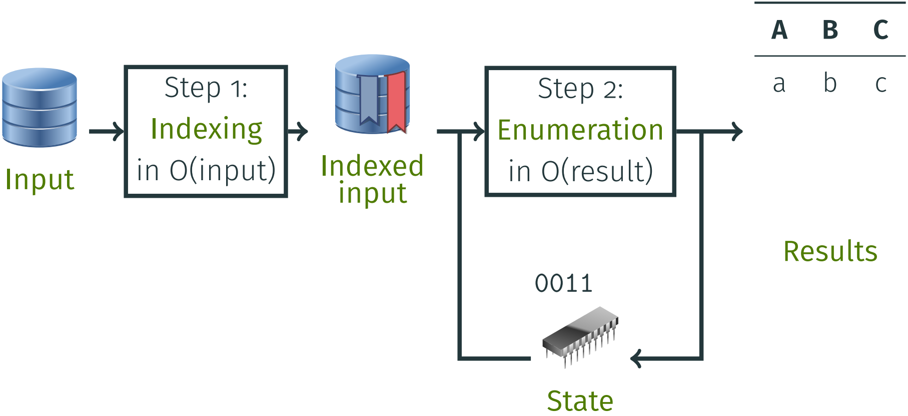

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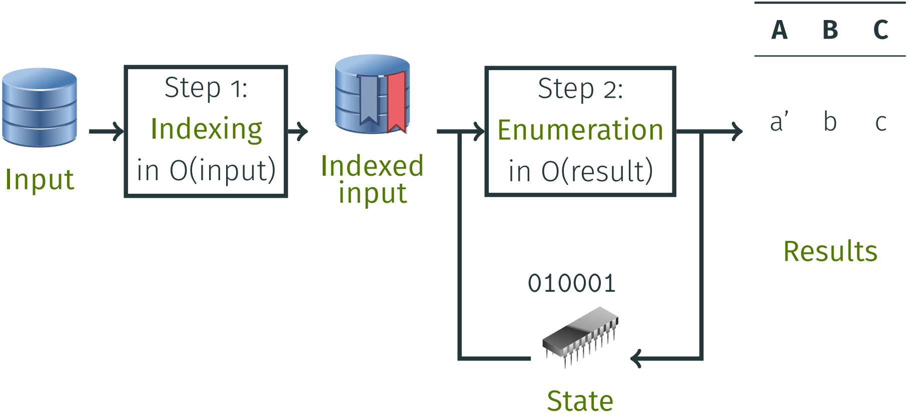

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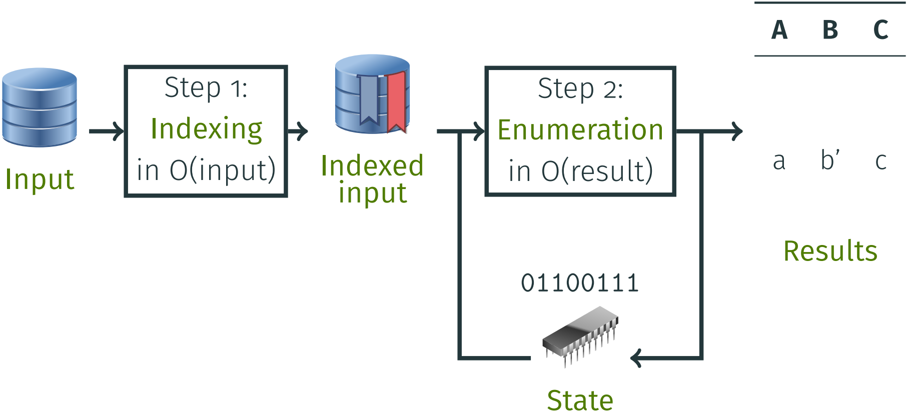

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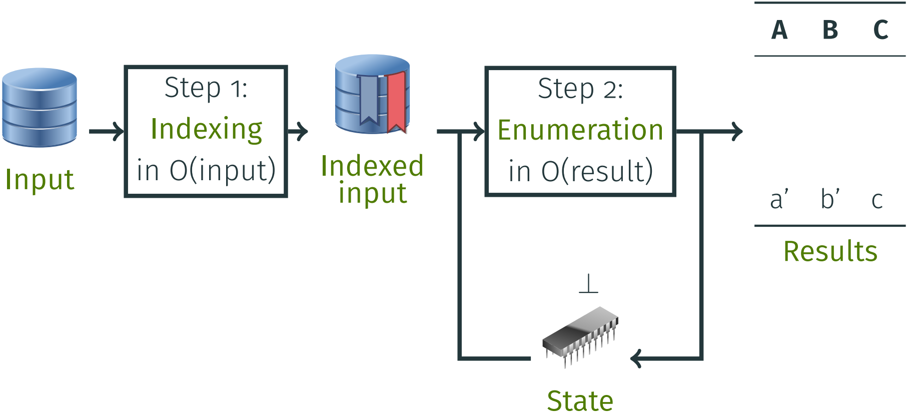

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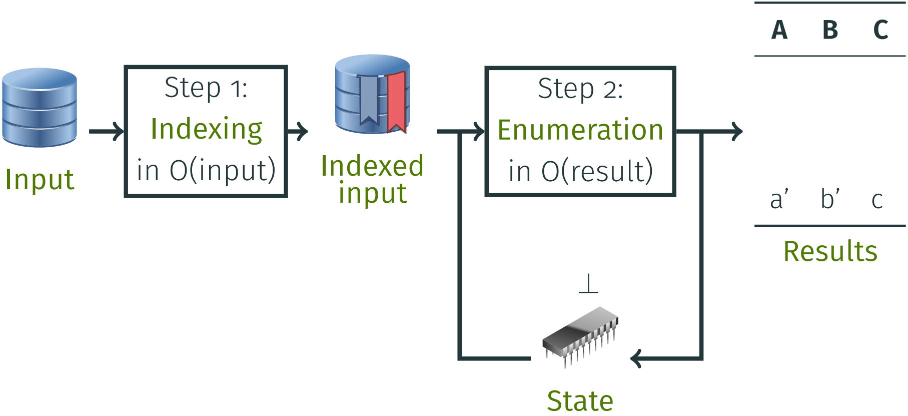
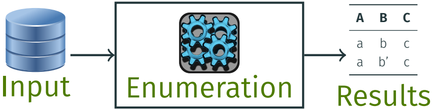


Important: every result computed exactly once

General idea for enumeration

Currently:



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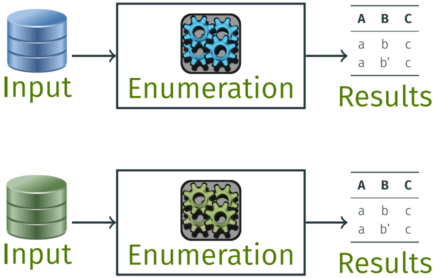

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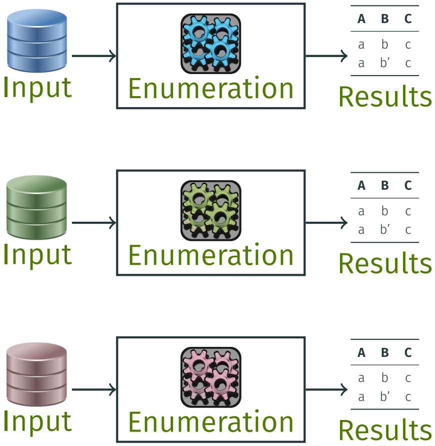

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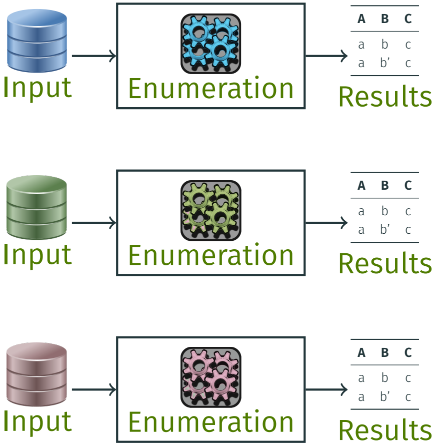

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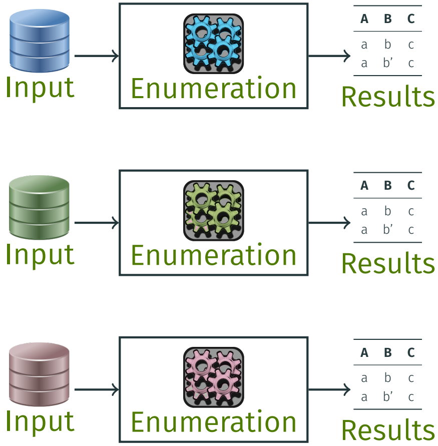

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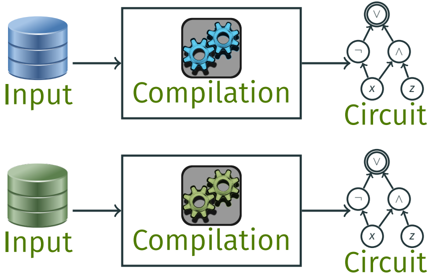

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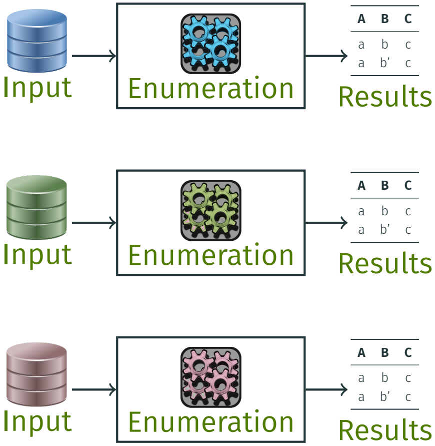

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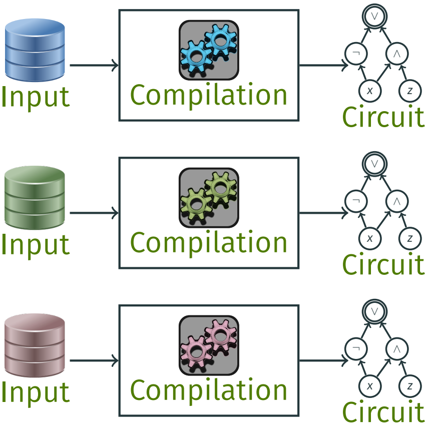

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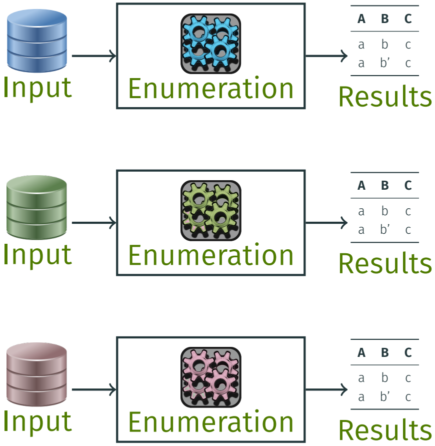

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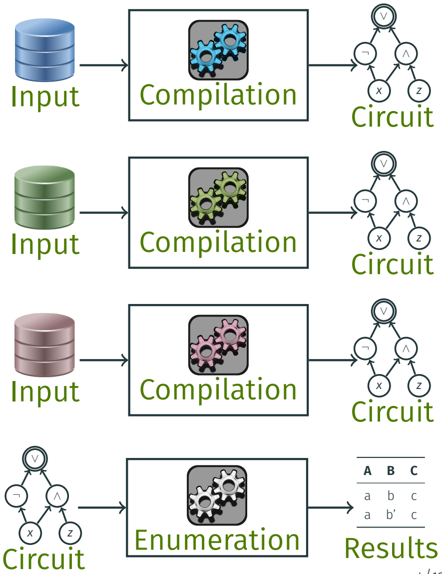
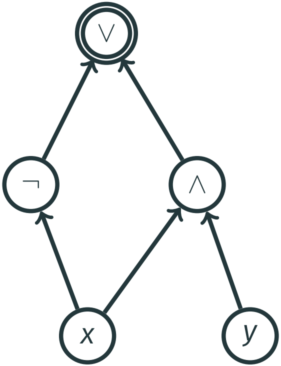
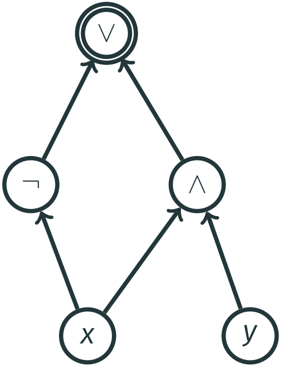


Boolean circuits



- Directed acyclic graph of gates

Boolean circuits



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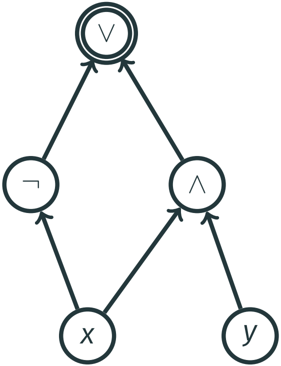

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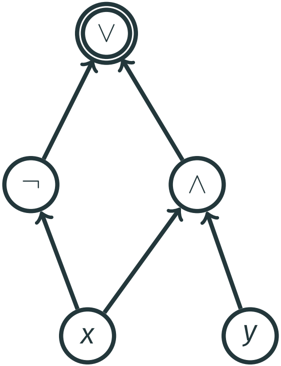

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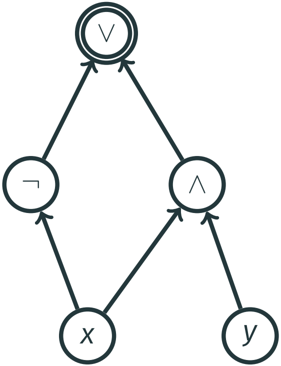

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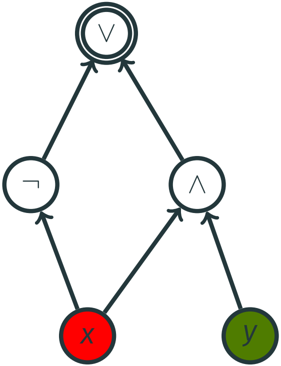

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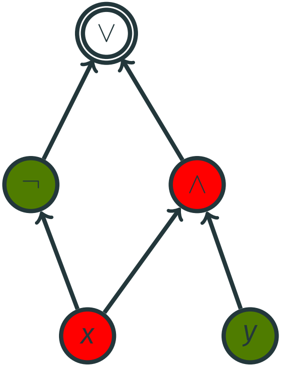

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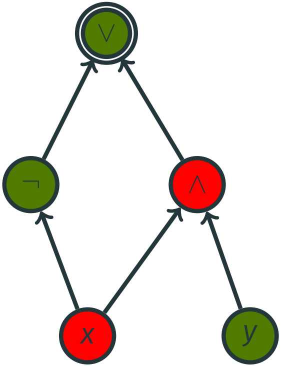

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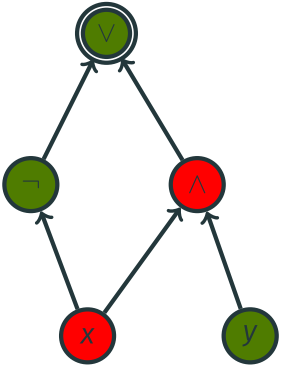

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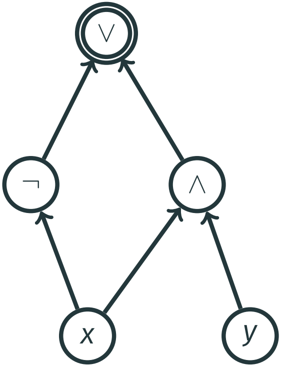

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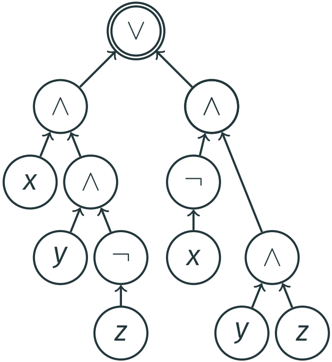
Our task: Enumerate all **satisfying assignments** of an input circuit

Circuit restrictions

d-DNNF:

- (∨) are all deterministic:

The inputs are mutually exclusive
(= no valuation ν makes two inputs
simultaneously evaluate to 1)



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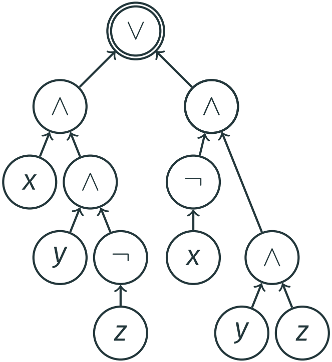

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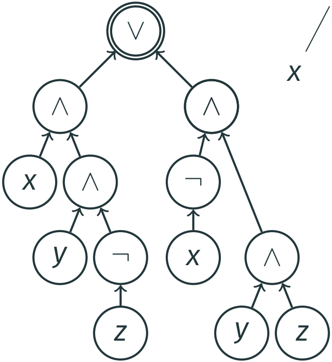
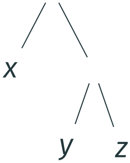
v-tree: ∧-gates follow a tree on the variables





Main results

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Also: restrict to assignments of constant size $k \in \mathbb{N}$ (at most k variables are set to 1):

Theorem

Given a d-DNNF circuit C with a v-tree T, we can enumerate its satisfying assignments of size $\leq k$ with preprocessing linear in $|C|$ and constant delay

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- Factorized databases: succinct representation of database tables

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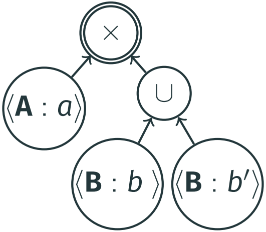

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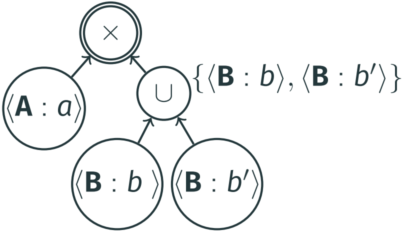

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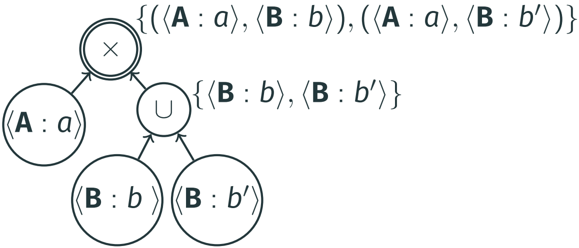

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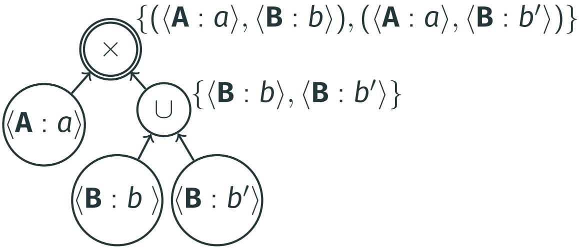

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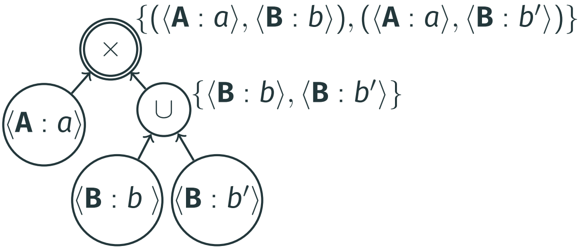

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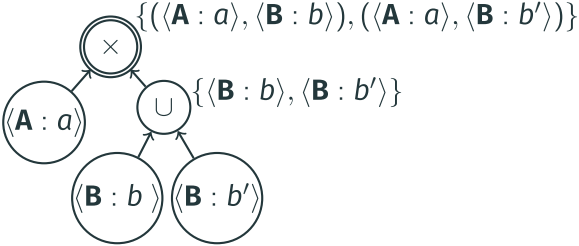

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Theorem (Strenghtens result of [Olteanu and Závodný, 2015])
Given a deterministic factorized representation, we can enumerate its tuples with linear preprocessing and constant delay

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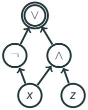
Theorem (Recaptures [Bagan, 2006], [Kazana and Segoufin, 2013])
For any constant $k \in \mathbb{N}$ and fixed MSO query Q, given a database D of treewidth $\leq k$, the results of Q on D can be enumerated with linear preprocessing in D and linear delay in each answer ($\rightarrow$ constant delay for free first-order variables)

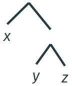
Proof techniques

Proof overview

Preprocessing phase:



Circuit



v-tree

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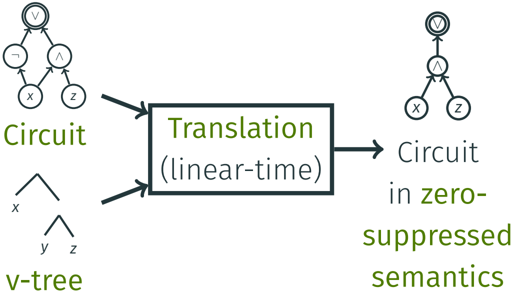

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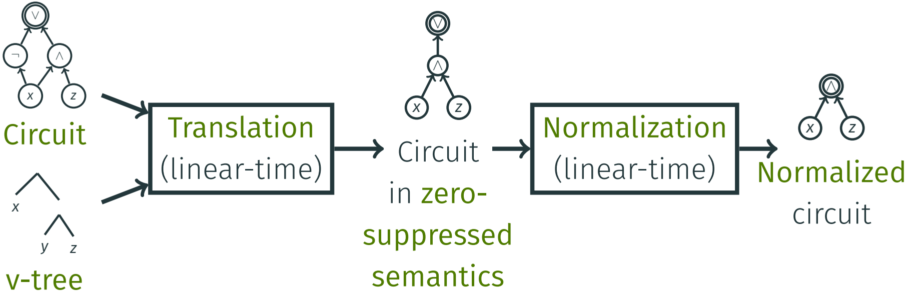

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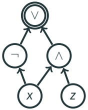

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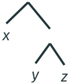
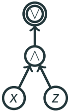


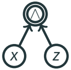
v-tree

→ **Translation** (linear-time) →



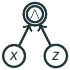
Circuit in zero-suppressed semantics

→ **Normalization** (linear-time) →



Normalized circuit

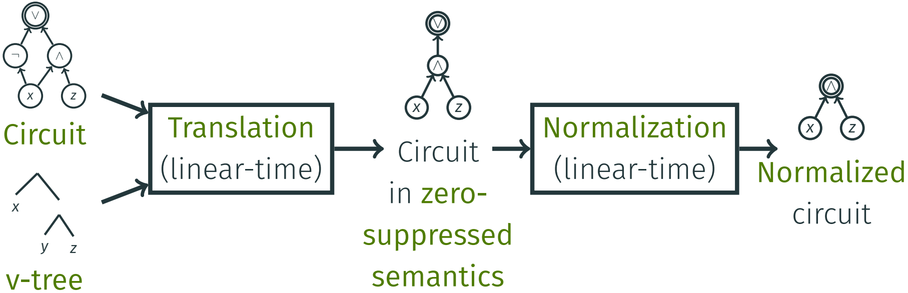
Enumeration phase:



Normalized circuit

Proof overview

Preprocessing phase:



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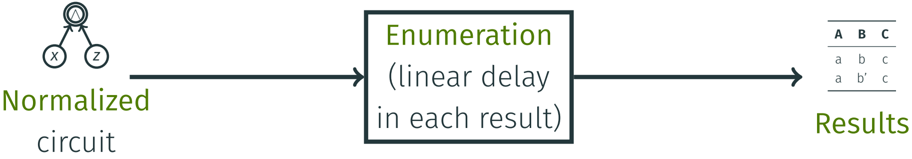
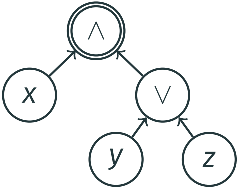
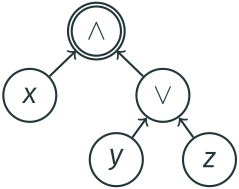


Zero-suppressed semantics



Special zero-suppressed semantics for circuits:

Zero-suppressed semantics



Special zero-suppressed semantics for circuits:

- No NOT-gate
- Each gate captures a set of assignments
- Bottom-up definition with $\times$ and $\cup$

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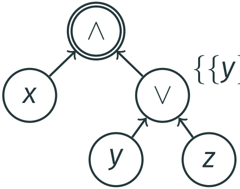

$\{\{y\}, \{z\}\}$

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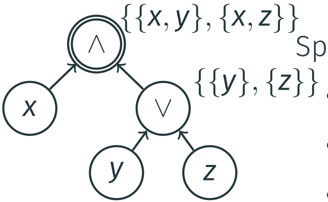

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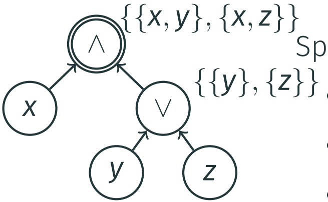

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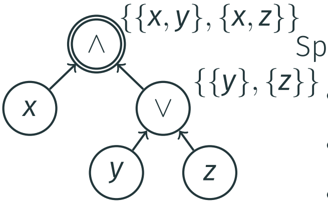

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Many equivalent ways to understand this:

- Generalization of factorized representations
- Generalization of zero-suppressed OBDDs (implicit negation)
- Arithmetic circuits: $\times$ and $+$ on polynomials

Enumerating assignments in the zero-suppressed semantics

Task: Enumerate the elements of the set $S(g)$ captured by a gate g

$\rightarrow$ E.g., for $S(g) = \{\{x, y\}, \{x, z\}\}$, enumerate $\{x, y\}$ and then $\{x, z\}$

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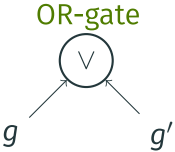

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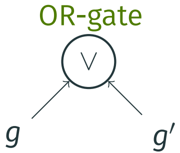

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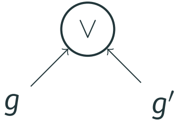
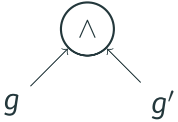
OR-gate



AND-gate



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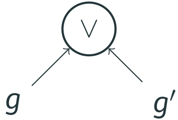

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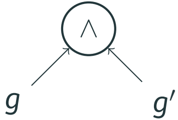

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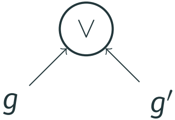

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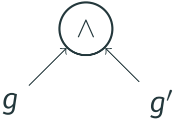

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- some technical problems →normalization necessary

Conclusion

Summary and conclusion

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Thanks for your attention!

References

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